REMARKS

Claims 1-36 are pending in the Application.

Claims 1-3, 4-7, 11-15, 16-19, 23, 24-28 and 31 stand rejected.

Claims 8-10, 20-22, 30 and 32-36 are objected.

Applicants have faxed an Applicant Initiated Interview Request Form on October 8, 2003. Applicants left several voice messages with Examiner Vu regarding receipt of the Interview Request Form. On October 13, 2003, Applicants were able to contact Examiner Vu. Examiner Vu informed Applicants that she did not have time to grant an interview with Applicants.

I. REJECTIONS UNDER 35 U.S.C. § 102(b):

Claims 24-28 and 31 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Orr et al. (U.S. Patent No. 4,862,350) (hereinafter "Orr").

For a claim to be anticipated under 35 U.S.C. § 102(b), each and every claim limitation must be found within the cited prior art reference and arranged as required by the claim. M.P.E.P. § 2131.

Orr does not disclose "issuing a plurality of commands by a processing unit to a direct memory access controller to be executed during one or more remote procedure calls" as recited in claim 24. The Examiner cites Figure 1, column 1, lines 17-25 and column 5, lines 27-34 of Orr as disclosing the above-cited claim limitation. Applicants respectfully disagree. Instead, Orr discloses:

> The rapid development and production of microprocessors have revolutionized the way in which multiprocessing systems are configured. Such multiprocessing systems use a plurality of microprocessors for performing the overall data processing functions. Each microprocessor is assigned a dedicated task while at least one of the microprocessors is assigned the task of correlating the results generated from each of the processors. Column 1, lines 17-25.
>
> These microprocessors are dedicated to perform specific tasks and periodically are given the opportunity to report their status or transfer information over the I/O link 36 to the shared buffer. Likewise,

> information for these devices is deposited in the shared buffer from the primary processor and is subsequently transmitted under the control of master processor 32 to the respective device. Column 5, lines 26-34.

Thus, Orr discloses a primary processor that transmits messages to a shared memory means and not to a direct memory access controller. Further, Orr is silent regarding a remote procedure call. Thus, Orr does not disclose all of the limitations of claim 24, and thus Orr does not anticipate claim 24.

Orr does not disclose "wherein said plurality of commands comprise a first instruction to copy attached processing unit instructions associated with a particular attached processing unit from a memory to said particular attached processing unit, wherein said plurality of commands comprise a second instruction to copy data associated with said attached processing unit instructions from said memory to said particular attached processing unit" as recited in claim 24. The Examiner cites column 5, lines 26-34 and column 11, lines 5-12 and 49-62 of Orr as disclosing the above-cited claim limitations. Applicants respectfully traverse. Instead, Orr discloses:

> These microprocessors are dedicated to perform specific tasks and periodically are given the opportunity to report their status or transfer information over the I/O link 36 to the shared buffer. Likewise, information for these devices is deposited in the shared buffer from the primary processor and is subsequently transmitted under the control of master processor 32 to the respective device. Column 5, lines 27-34.

> The transmit message parameters consist of three bytes located at 80286 memory location 080005-080007. These bytes are read by the master 8051 whenever bit 4 of the request byte is set. The first byte tells the 8051 how many transmit messages there are in the buffer. The next two bytes point to the address in the message space where the first byte of the first message entry is located. Column 11, lines 5-12.

> The message space is a space in the shared buffer where messages are placed to be transmitted or are placed when received by the master 8051. The space is defined in 80286 memory address location 08012B-08007FF. Messages in this space are pointed to by the appropriate transmit/receive message parameters previously described. All messages received by the master 8051 from I/O devices are placed in this area and the appropriate receive message pointer is generated. When the 80286 has messages to transmit, they are placed in this

> space and the appropriate transmit message parameters generated. If the 80286 has more than one message to transmit, they must be placed in the message space in continuous memory locations. Column 11, lines 49-62.

Thus, Orr discloses a primary processor depositing information for devices in a shared buffer which is subsequently transmitted to the respective device by a master processor. This language does not disclose an instruction to copy attached processing unit instructions from a memory to a particular attached processing unit. Instead, the information provided by the primary processor relates to information that is used by the respective device to perform their specific task, e.g. print, scan a document, display an image. Further, Orr discloses message parameters which may indicate how many transmit messages are in the buffer. Orr further discloses that the shared buffer includes a message space to hold messages that have to be transmitted or placed by the master processor. However, this language does not disclose a command that includes a second instruction to copy data from a memory to a particular attached processing unit. Thus, Orr does not disclose all of the limitations of claim 24, and thus Orr does not anticipate claim 24.

Orr does not disclose "issuing to said particular attached processing unit an indication to start a particular operation on said data associated with said particular attached processing unit instructions" as recited in claim 24. The Examiner cites column 11, lines 42-48 of Orr as disclosing the above-cited claim limitation. Applicants respectfully traverse. Instead, Orr discloses:

> The list is downloaded into the shared buffer and the master 8051 accesses the list sequentially and depending on the address of the device in the list a poll is generated and transmitted to the device. As a result of the poll, the device is given an opportunity to transmit data to the shared buffer. Column 11, lines 42-48.

Thus, Orr discloses a poll list that includes a list of the devices which are attached to the system. The poll list is downloaded into the shared buffer and the master processor accesses the list sequentially, and depending on matters of the device in the list, a poll is generated and transmitted to the device. Orr further discloses that, as a result of the poll, the device is given an opportunity to transmit data to the shared

buffer. This language does not disclose issuing to a particular attached processing unit an indication to start an operation on the data. Further, this language does not disclose that the data is associated with particular attached processing unit instructions. Thus, Orr does not disclose all of the limitations of claim 24, and thus Orr does not anticipate claim 24.

Orr does not disclose "wherein said plurality of attached processing units do not interrupt said processing unit upon completion of each of said one or more remote procedure calls" as recited in claim 24. The Examiner cites the abstract and column 3, lines 12-20 of Orr as disclosing the above-cited claim limitation. As stated above, Orr discloses that the devices coupled to a master processor via an I/O link may be given the opportunity to transmit data into a shared memory means via the master processor. Orr further discloses that the messages placed in the shared memory means may be accessed by a primary processor. However, this language does not disclose remote procedure calls. Hence, Orr does not disclose an attached processing unit not interrupting a processing unit upon completion of a remote procedure call. Thus, Orr does not disclose all of the limitations of claim 24, and thus Orr does not anticipate claim 24.

Claims 25-28 and 31 each recite combinations of features including the above combinations, and thus are not anticipated for at least the above stated reasons. Claims 25-38 and 31 recite additional features, which, in combination with the features of the claims upon which they depend, are not anticipated by Orr.

For example, Orr does not disclose "wherein said attached processing unit instructions enable said particular attached processing unit to perform said particular operation" as recited in claim 25. The Examiner cites column 5, lines 26-34 of Orr as disclosing the above-cited claim limitation. Instead, as stated above, Orr discloses that the primary processor deposits information for devices in a shared buffer which is subsequently transmitted by a master processor to the respected device. Orr is silent regarding what constitutes this information that is deposited in a shared buffer. That is, Orr is silent as to whether the information constitutes instructions that enable

a device to perform a particular operation. Thus, Orr does not disclose all of the limitations of claim 25, and thus Orr does not anticipate claim 25.

Orr does not disclose "interrupting said processing unit at a synchronization point, wherein said synchronization point occurs after said one or more remote procedures calls are performed" and recited in claim 27. The Examiner cites column 7, lines 6-29 of Orr as disclosing the above-cited claim limitation. Instead, Orr discloses:

> Still referring to FIG. 2, the handshaking and control for the accessing of the shared memory is done through control interface 44. The control interface 44 includes latches L1, L3 and L2. Latches L1 and L3 are connected by conductor 54 to a combinatorial logic means identified as Al. Combinatorial logic means A1 is tied to the address bus of primary processor 10. Similarly, latches L3 and L2 are tied by conductor 56 to combinatorial logic means A2. Combinatorial logic means A2 is tied to the address bus of master processor 32. An interrupt control line identified by numeral 58 interconnects primary processor 10 to the control interface 44 while an interrupt control line identified by numeral 60 interconnects master processor 32 to control interface 44. As will be explained subsequently, these interrupt lines are activated when either of the processors requires use of the shared message buffer. A control line identified by numeral 61 interconnects the control interface 44 with tri-state buffers D1 and D2, respectively. An inverter circuit identified by numeral 62 interconnects the enable line to tri-state buffer D3. This inverter insures that the electrical state of D1, D2 is opposite to the electrical state of D3, D4. Stated another way, when D1 and D2 are enabled, D3 and D4 are disabled and vice versa. Column 7, lines 6-29.

Thus, Orr discloses a control interface that controls ownership of the shared memory means between the primary processor and the master processor via handshaking. However, this language does not disclose a synchronization point that occurs after one or more remote procedure calls are performed. As stated above, Orr is silent regarding a remote procedure call. Thus, Orr does not disclose all of the limitations of claim 27, and thus Orr does not anticipate claim 27.

Orr does not disclose "wherein said direct memory access controller comprises a plurality of first level queues for storing said plurality of commands" as recited in claim 28. The Examiner cites column 9, lines 26-59 and column 11,

lines 49-62 of Orr as disclosing the above-cited claim limitation. Instead, Orr discloses:

> In the preferred embodiment of this invention the message buffer is a 2K.times.8 static RAM used to pass messages and status commands between the primary processor 10 and the master processor 32. As stated above, in the preferred embodiment of the invention the primary processor is an Intel 80286 processor while the master processor is an Intel 8051 processor. When a message is to be transmitted to an I/O device, the 80286 places the message in the message buffer and the master 8051 sends the message out over the serial I/O link. When a message is received from an I/O device, the master 8051 places the message in the message buffer. The 80286 is then notified that there is a received message in the message buffer which should be moved to the 80286 non-shared memory space. Column 9, lines 26-40.
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> The message space is a space in the shared buffer where messages are placed to be transmitted or are placed when received by the master 8051. The space is defined in 80286 memory address location 08012B-08007FF. Messages in this space are pointed to by the appropriate transmit/receive message parameters previously described. All messages received by the master 8051 from I/O devices are placed in this area and the appropriate receive message pointer is generated. When the 80286 has messages to transmit, they are placed in this space and the appropriate transmit message parameters generated. If the 80286 has more than one message to transmit, they must be placed in the message space in continuous memory locations. Column 11, lines 49-62.

Thus, Orr discloses that the shared buffer is divided into different functional areas where one functional area is a place for messages to be received from the master processor which were received from the devices connected to the master processor via the I/O link. Orr further discloses that another functional area in the shared memory buffer is a place to store messages that were transmitted from the primary processor. These messages will later be retrieved by the master processor and delivered to the devices connected to the master processor via the I/O link. These messages are stored in a shared memory buffer which is the shared memory means 20. Shared memory means 20 is <u>not</u> a part of a direct memory access controller. Hence, Orr does not disclose a direct memory access controller that

comprises a plurality of first level queues for storing commands. Thus, Orr does not disclose all of the limitations of claim 28, and thus Orr does not anticipate claim 28.

Orr does not disclose "wherein said first and second instructions to copy attached processing unit instructions and data associated with said attached processing unit instructions are requests to copy one or more lines in said memory to said particular attached processing unit" as recited in claim 31. The Examiner cites column 11, lines 5-12 and lines 49-62 of Orr as disclosing the above-cited claim limitation. Paper No. 5, page 3. Instead, as stated above, Orr discloses that the shared buffer is divided into different functional areas including an area designated to receive messages transmitted from the primary processor and a designated area to receive messages retrieved from the master processor that were transmitted from the device connected to the master processor via an I/O link. This language does not disclose instructions that are requests to copy one or more lines in memory to a particular attached processing unit. Orr is silent regarding the contents of these messages that are stored in the shared buffer. Thus, Orr does not disclose all of the limitations of claim 31, and thus Orr does not anticipate claim 31.

As a result of the foregoing, Applicants respectfully assert that not each and every claim limitation is found within the cited prior art reference, and thus claims 24-28 and 31 are not anticipated by Orr.

II. REJECTIONS UNDER 35 U.S.C. § 103(a):

Claims 1-2, 4-7, 11-14, 16-19 and 23 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Orr in view of Applicant's admitted prior art (hereinafter "AAPA"). Claims 3, 15 and 29 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Orr in view of AAPA and in further view of Goyal et al. (U.S. Patent No. 6,055,579) (hereinafter "Goyal").

A. The Examiner has not provided any motivation for modifying Orr with AAPA.

A *prima facie* showing of obviousness requires the Examiner to establish, *inter alia*, that the prior art references teach or suggest, either alone or in

combination, all of the limitations of the claimed invention, and the Examiner must provide a motivation or suggestion to combine or modify the prior art reference to make the claimed inventions. M.P.E.P. § 2142. The motivation or suggestion to combine references must come from one of three possible sources: the nature of the problem to be solved, the teaching of the prior art and the knowledge of persons of ordinary skill in the art. *In re Rouffet*, 47 U.S.P.Q. 2d. 1453,1458 (Fed. Cir. 1998). The showings must be clear and particular. *In re Lee*, 277 F. 3d 1338, 1343, 61 U.S.P.Q. 2d 1430, 1433-34 (Fed. Cir. 2002); *In re Kotzab*, 217 F. 3d 1365, 1370, 55 U.S.P.Q. 2d 1313, 1317 (Fed. Cir. 2000); *In re Dembiczak*, 50 U.S.P.Q. 2d. 1614, 1617 (Fed. Cir. 1999). Broad conclusory statements regarding the teaching of multiple references, standing alone, are not evidence. *Id.*

The Examiner states:

> However, Orr does not explicitly disclose the system comprises a plurality of processing elements. AAPA teaches a system with a plurality of processing elements (SMP) (page 2). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement multiple processing elements as taught by AAPA in the system of Orr to improve the processing speed and transaction throughput. Paper No. 5, pages 4-5.

Thus, the Examiner's motivation for modifying Orr to have a system comprising "a plurality of processing elements coupled to said shared memory," as reciting claim 1, is that it would have been obvious to one of ordinary skill in the art "to improve the processing speed and transaction throughput." Paper No. 5, page 5. The Examiner's statement above is not supported by any objective evidence.

As stated above, Orr teaches a single primary processor that deposits information in a shared memory means that is later retrieved by a master processor and subsequently transmitted to remote devices via an I/O link coupled to the master processor. The Examiner has not shown why Orr should be modified to have a plurality of primary processors coupled to the shared memory means. The Examiner must submit **objective evidence** and not rely on her own subjective opinion in support of modifying Orr to have a plurality of primary processors coupled to a

shared memory means. *In re Lee*, 61 U.S.P.Q.2d 1430, 1434 (Fed. Cir. 2002). Therefore, the Examiner has not presented a *prima facie* case of obviousness for rejecting claims 1-2, 4-7, 11-14, 16-19 and 23.

B. *Orr and AAPA, taken singly or in combination, do not teach or suggest the following limitations.*

Orr and AAPA, taken singly or in combination, do not teach or suggest "a plurality of processing elements coupled to said shared memory" as recited in claim 1 and similarly in claim 13. As stated above, the Examiner must submit **objective evidence** and not rely on her own subjective opinion in support of modifying Orr to have a plurality of processing elements coupled to a shared memory. *In re Lee*, 61 U.S.P.Q. 2d 1430, 1434 (Fed. Cir. 2002). Accordingly, the Examiner has not presented a *prima facie* case of obviousness for rejecting claims 1 and 13. M.P.E.P. § 2143.

Orr and AAPA, taken singly or in combination, do not teach or suggest "wherein said direct memory access controller is configured to receive a plurality of commands from a corresponding processing unit to be executed during one or more remote procedure calls" as recited in claim 1 and similarly in claim 13. The Examiner cites column 5, lines 26-34 of Orr as teaching the above-cited claim limitation. Instead, as stated above, Orr teaches a primary processor depositing information in a shared memory means that will later be retrieved by a control processor to be delivered to a particular device via an I/O serial link. However, this language is silent regarding the primary processor depositing information during a remote procedure call. Further, the primary processor is depositing information in the shared memory means and not to the master processor. That is, the master processor is not receiving the information from the primary processor but instead retrieves it from the shared memory means. Hence, this language does not teach or suggest a direct memory access controller configured to receive a plurality of commands from a processing unit to be executed during one or more remote procedure calls. Therefore, the Examiner has not presented a *prima facie* case of obviousness for rejecting claims 1 and 13. M.P.E.P. § 2143.

Orr and AAPA, taken singly or in combination, do not teach or suggest "wherein each of said plurality of attached processing units in each of said plurality of processing elements does not interrupt said corresponding processing unit upon completion of each of said one or more remote procedure calls" as recited in claim 1. The Examiner cites the abstract and column 3, lines 12-20 of Orr as teaching the above-cited claim limitation. Instead, as stated above, Orr teaches a primary processor that places messages in a shared memory that is later retrieved and transmitted to a particular remote device. However, as stated above, this language is silent regarding a remote procedure call. Hence, this language does not teach or suggest an attached processing unit that does not interrupt a corresponding processing unit upon a completion of a remote procedure call. Therefore, the Examiner has not presented a *prima facie* case of obviousness for rejecting claim 1. M.P.E.P. § 2143.

Claims 2, 4-7, 11-12, 14, 16-19 and 23 recite combinations of features including the above combinations, and thus they are patentable for at least the above stated reasons. Claims 2, 4-7, 11-12, 14, 16-19 and 23 recite additional features, which, in combination with the features of the claims upon which they depend, are patentable over Orr in view of AAPA.

For example, Orr and AAA, taken singly or in combination, do not teach or suggest "wherein said direct memory access controller in each of said plurality of processing elements comprises a plurality of first level queues for storing said plurality of commands issued by said corresponding processing unit" as recited in claim 2 and similarly in claim 14. The Examiner cites column 9, lines 26-59 and column 11, lines 49-62 of Orr as teaching the above-cited claim limitation. Instead, as stated above, Orr teaches that the shared memory means, i.e., shared buffer, is divided up into different functional areas. One functional area is designated to receive messages from the primary processor and another functional area is designated to receive messages from the master processor. The shared buffer is not located in a direct memory access controller but is instead located separate from the master processor. Hence, Orr does not teach or suggest a direct memory access controller that comprises a plurality of first level queues for storing a plurality of

commands issued by a processing unit. Therefore, the Examiner has not presented a *prima facie* case of obviousness for rejecting claims 2 and 14. M.P.E.P. § 2143.

Orr and AAPA, taken singly or in combination, do not teach or suggest "wherein said plurality of commands comprise a first instruction to copy attached processing unit instructions associated with a particular attached processing unit from said shared memory to said particular attached processing unit, wherein said plurality of commands comprise a second instruction to copy data associated with said attached processing unit instructions from said shared memory to said particular attached processing unit" as recited in claim 4 and similarly in claim 16. The Examiner cites column 5, lines 26-34 and column 11, lines 5-12 and 49-62 of Orr as teaching the above-cited claim limitations. Instead, as stated above, Orr teaches that a primary processor may deposit information in a shared buffer that is later retrieved and transmitted by a master processor to a remote device. The shared buffer is divided into functional areas where one function area may be designated to receive messages from the primary processor and another area may be designated to retrieve messages from the master processor. However, this language is silent regarding whether the information deposited by the primary processor in the shared buffer is a command to copy processing unit instructions from a shared memory to a particular processing unit or an instruction to copy data associated with a processing unit instruction from a shared memory to a particular attached processing unit. Hence, Orr does not teach or suggest a plurality of commands issued by a processing unit that includes an instruction to copy attached processing unit instructions associated with a particular attached processing unit from a shared memory to a particular attached processing unit as well as including an instruction to copy data associated with an attached processing unit instruction from the shared memory to a particular attached processing unit. Therefore, the Examiner has not presented a *prima facie* case of obviousness for rejecting claims 4 and 16. M.P.E.P. § 2143.

Orr and AAPA, taken singly or in combinations, do not teach "wherein said attached processing unit instructions associated with said particular attached processing unit comprise instructions that enable said particular attached processing unit to perform a particular operation on said data associated with said attached

processing unit instructions associated with said particular attached processing unit" as recited in claim 5 and similarly in claim 17. The Examiner cites column 5, lines 26-34 of Orr as teaching the above-cited claim limitation. Instead, as stated above, Orr teaches a primary processor that deposits information in a shared buffer that is later retrieved and transmitted by a master processor to a remote device. However, Orr is silent regarding what constitutes the information deposited by the primary processor. That is, Orr is silent regarding whether the information deposited by the primary processor is an instruction that enables a remote device to perform a particular operation on data. Therefore, the Examiner has not presented a *prima facie* case of obviousness for rejecting claims 5 and 17. M.P.E.P. § 2143.

Orr and AAPA, taken singly or in combination, do not teach or suggest "wherein said plurality of commands comprise a third instruction to copy the results of said particular operation to said shared memory" as recited in claims 6 and 18. The Examiner cites column 5, lines 49-58 of Orr as teaching the above-cited claim limitation. Instead, Orr teaches:

> In operation, the plurality of remote microprocessor control devices perform specific tasks and transport the information over communication channel 36 to primary processor 10. The primary processor performs some central processing function returning results to a selected remote processor and/or a higher level processor. A message buffer 20 under the control of a master processor 32 is used to facilitate the exchange of messages and data between the remote processors and the primary processor. When the described distributed architecture of the present invention is used in a point of sale terminal, the main terminal includes the primary processor, the shared buffer, the master processor, the plurality of microprocessor control devices 22-30, and the feature cards 46. Column 5, lines 49-63.

Thus, Orr teaches that the remote devices perform a specific task and transport that information to the primary processor via the master processor. The primary processor then performs a function on this information and returns the results to a selected remote processor and/or higher level processor. However, this language is silent regarding a processing unit issuing a command to the direct memory access controller to copy the results of a particular operation to a shared memory. Orr is silent

regarding an instruction to copy the results of an operation performed by a remote device to the shared memory. Therefore, the Examiner has not presented a *prima facie* case of obviousness for rejecting claims 6 and 18. M.P.E.P. § 2143.

Orr and AAPA, taken singly or in combination, do not teach or suggest "wherein said first and second instructions to copy attached processing unit instructions and data associated with said attached processing unit instructions are requests to copy one or more lines of memory in said shared memory to said particular attached processing unit" as recited in claim 7 and similarly in claim 19. The Examiner cites column 11, lines 5-12 and 49-62 of Orr as teaching the above-cited claim limitation. Instead, as stated above, Orr teaches a shared buffer that is divided into functional areas. One functional area may be designated to receive messages transmitted from a primary processor. Another function area may be designated to receive messages transmitted from a master processor. However, Orr is silent regarding the primary processor transmitting requests to copy one or more lines of memory in the shared memory to a particular attached processing unit. Therefore, the Examiner has not presented a *prima facie* case of obviousness for rejecting claims 7 and 19. M.P.E.P. § 2143.

Orr and AAPA, taken singly or in combination, do not teach or suggest "wherein said direct memory access controller is configured to interrupt said corresponding processing unit at a synchronization point, wherein said synchronization point occurs after said one or more remote procedure calls are performed" as recited in claim 12 and similarly in claim 23. Examiner cites column 7, lines 6-29 of Orr as teaching the above-cited claim limitation. As stated above, Orr teaches a control interface that controls ownership of the shared memory means between the primary processor and the master processor via handshaking. However, this language does not teach a synchronization point that occurs after one or more remote procedure calls are performed. As stated above, Orr is silent regarding a remote procedure call. Therefore, the Examiner has not presented a *prima facie* case of obviousness for rejecting claims 12 and 23. M.P.E.P. § 2143.

C. *The Examiner has not provided any motivation for combining Orr with AAPA and Goyal.*

As stated above, a *prima facie* showing of obviousness requires the Examiner to establish, *inter alia*, that the prior art references teach or suggest, either alone or in combination, all of the limitations of the claimed invention, and the Examiner must provide a motivation or suggestion to combine or modify the prior art reference to make the claimed inventions. M.P.E.P. §2142. The motivation or suggestion to combine references must come from one of three possible sources: the nature of the problem to be solved, the teaching of the prior art and the knowledge of persons of ordinary skill in the art. *In re Rouffet*, 47 U.S.P.Q. 2d. 1453,1458 (Fed. Cir. 1998). The showings must be clear and particular. *In re Lee*, 277 F. 3d 1338, 1343, 61 U.S.P.Q. 2d 1430, 1433-34 (Fed. Cir. 2002); *In re Kotzab*, 217 F. 3d 1365, 1370, 55 U.S.P.Q. 2d 1313, 1317 (Fed. Cir. 2000); *In re Dembiczak*, 50 U.S.P.Q. 2d. 1614, 1617 (Fed. Cir. 1999). Broad conclusory statements regarding the teaching of multiple references, standing alone, are not evidence. *Id.*

The Examiner states:

> As to claims 3 and 15, Orr and AAPA do not explicitly teach each of said plurality of first level queues are configured to store one or more commands of said plurality of commands associated with a different attach processing unit. Goyal teaches a plurality of command queues wherein each of the command queues is to store the commands associated with different attached processing unit (processing engines) (col. 10, lines 55-62). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement a plurality of command queues wherein each queue is configured to store the commands associated with different processing engine as taught by Goyal in a system of Orr and AAPA so that the processing activities of each of the processing engine are efficiently coordinated for optimal data throughput with minimum idling of processing engines, software processing overhead and latency (col. 4, lines 15-26). Paper No. 5, page 7.

Thus, the Examiner's motivation for modifying Orr to have a direct memory access controller include a plurality of first level queues where each of the plurality of first level queues are configured to store one or more commands associated with a different attached processing unit, as recited in claims 3, 15 and 29, is "so that the

processing activities of each of the processing engines are efficiently coordinated for optimal data throughput with minimum idling of processing engines, software processing overhead and latency." Paper No. 5, page 7. This is merely the Examiner's own opinion which does not amount to the required objective evidence to support a *prima facie* case of obviousness.

Further, there is no motivation to combine Orr with Goyal. In particular, there is no suggestion or motivation in either Orr or Goyal, or in their combination, or in the knowledge of those ordinarily skilled in the art to combine the teaching of an architecture for interconnecting the plurality of remote processors to a primary processor, as taught in Orr, with the teaching of processing data using unconditional and conditional queuing of processing commands in one or more queues for one or more processing engines in a data processing system, as taught in Goyal.

As stated above, Orr teaches a primary processor that deposits messages in a shared buffer that is later retrieved and transmitted to remote devices by a master processor.

Goyal, on the other hand teaches:

> A system for synchronization of data processing in a data processing system including multiple command queues is disclosed. The disclosed data processing system includes one or more processing engines associated with one or more command queues. The use of multiple command queues supports multiple priority levels, such that commands in higher priority queues may preempt commands in lower priority queues. Data processing is synchronized by queue commands that allow a processing engine to queue commands on the command queue of any processing engine in the data processing system, including its own. Multiple data dependencies are resolved by conditional queue commands and event counters that queue a command only when all of the conditions precedent to execution of a particular data processing command are satisfied. The hardware queuing of the disclosed invention advantageously synchronizes data processing with minimal software supervision and with minimal latency. Abstract.

Thus, Goyal teaches a system for synchronization of data processing in a data processing system that includes multiple command queues. Goyal further teaches one or more processing engines associated with one or more command queues.

The Examiner has not shown why a reference that teaches an architecture for interconnecting a plurality of remote processors to a primary processor, as taught in Orr, should be combined with a reference that teaches using unconditional and conditional queuing of processing commands in one or more queues for one or more processing engines in a data processing system, as taught in Goyal. The Examiner must submit **objective evidence** and not rely on her own subjective opinion in support of combining the reference that teaches an architecture for interconnecting a plurality of remote processors to a primary processor with a reference that teaches processing of data using unconditional and conditional queuing of processing commands in one or more queues for one or more processing engines in the data processing system. *In re Lee*, 61 U.S.P.Q.2d 1430, 1434 (Fed. Cir. 2002) Therefore, the Examiner has not presented a *prima facie* case of obviousness for rejecting claims 3, 15 and 29.

As stated above, the Examiner's motivation for modifying Orr to have a direct memory access controller that comprises a plurality of first level queues which are configured to store one or more commands associated with a different attached processing unit is so that the processing activities of each of the processing engines are efficiently coordinated for optimal data throughput with minimum idling of processing engines, software processing overhead and latency. Paper No. 5, page 7. The Examiner has not shown why Orr should be modified to have a direct memory access controller that comprises a plurality of first level queues which are configured to store one or more commands associated with a different attached processing unit. Further, the Examiner has not shown why Orr should be modified to have a plurality of processing engines where the processing activities of each of the processing engines are efficiently coordinated for optimal data throughput with minimum idling of processing engines, software processing overhead and latency.

The Examiner must submit **objective evidence** and not rely on her own subjective opinion in support of modifying Orr to have a direct memory access controller comprise a plurality of first level queues which are configured to store one or more commands associated with a different attached processing unit. *In re Lee*, 61 U.S.P.Q.2d 1430, 1434 (Fed. Cir. 2002). Further, the Examiner must submit **objective evidence** and not rely on her own subjective opinion in support of modifying Orr to have a plurality of processing engines where processing activities of each of the processing engines are efficiently coordinated for optimal data throughput with minimum idling of processing engines, software processing overhead and latency. *Id.* Accordingly, the Examiner has not presented a *prima facie* case of obviousness for rejecting claims 3, 15 and 29.

D. Orr, AAPA and Goyal, taken singly or in combination do not teach or suggest the following limitations.

Orr, AAPA and Goyal, taken singly or in combination, do not teach or suggest "wherein each of said plurality of first level queues are configured to store one or more commands of said plurality of commands associated with a different attached processing unit" as recited in claim 3 and similarly in claims 15 and 29. The Examiner cites column 10, lines 55-62 of Goyal as teaching the above-cited claim limitation. Instead, Goyal teaches:

> 1. A data processing system comprising:
> a host processor;
> a plurality of processing engines coupled to said host processor;
> a plurality of command queues capable of receiving, storing and retrieving a plurality of processing commands and queue management commands, each command queue associated with one of said plurality of processing engines.
> Column 10, lines 53-62.

Thus, Goyal teaches a plurality of command queues capable of receiving commands where each command queue is associated with a processing engine. However, these queues are not located in a direct memory access controller. Further, as stated above, Orr does not teach or suggest a direct memory access controller comprising a plurality of queues. Hence, Orr, AAPA and Goyal, taken singly or in combination, do not teach or suggest a direct memory access controller that comprises a plurality of

first level queues where each of the plurality of first level queues are configured to store one or more commands associated with a different attached processing unit. Therefore, the Examiner has not provided a *prima facie* case of obviousness for rejecting claims 3, 15 and 29. M.P.E.P. § 2143.

III. CONCLUSION

As a result of the foregoing, it is asserted by Applicants that claims 1-36 in the Application are in condition for allowance, and Applicants respectfully request an allowance of such claims. Applicants respectfully request that the Examiner call Applicants' attorney at the below listed number if the Examiner believes that such a discussion would be helpful in resolving any remaining issues.

Respectfully submitted,

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